REMARKS

By this Amendment, Applicant has canceled claim 18, amended claims 1, 3, 4, 8 and 17, and added claims 20-25. Claims 9-16 have been withdrawn from consideration. Claims 1-5, 7, 8, 17, 19 and 20-25 are pending in the application. In view of the above amendments and the following remarks, favorable reconsideration in this application is respectfully requested.

The Examiner rejected claims 1-3 and 7 under 35 U.S.C. 103(a) as being unpatentable over WO 00/12786 to Tamatsuka, translated as U.S. Patent No. 6,413,310. The Examiner also rejected claim 4 as being unpatentable over Tamatsuka in view of U.S. Patent No. 5,352,615 to Limb et al. ("Limb"), claim 5 as being unpatentable over U.S. Patent No. 4,376,657 to Nagasawa et al. ("Nagasawa") in view of U.S. Patent No. 4,429,047 to Jastrzebski et al. along with U.S. Patent No. 5,882,989 to Falster, claims 17-19 as being unpatentable over U.S. Patent No. 5,968,264 to Iida et al. ("Iida") in view of U.S. Patent No. 4,193,783 to Matsushita, and claim 8 as being unpatentable over Iida in view of Matsushita and further in view of Nagasawa.

As set forth in amended claim 1 and 8, and new claims 20 and 25, the present invention is directed to a method of treating a wafer thermally to remove grown-in defects contained in single crystalline semiconductor, having a step of carrying out a heat treatment on the wafer at a temperature equal to or higher than 1200 °C. The heat treatment is carried out either under a non-oxidative atmosphere (claims 1 and 8) or under an oxidative atmosphere (claims 20 and 25). After the heat treatment, an RTP annealing is carried out on the wafer at a temperature equal to or lower than 800°C for a period having a duration of two minutes or less.

Tamatsuka is directed to a method for producing a silicon single crystal wafer with high productivity by reducing COP grown-in defects in the silicon wafer layer. To achieve this object, the method of Tamatsuka grows a silicon single crystal ingot by the Cz method, slices the ingot into a wafer, subjects the wafer to a heat treatment at a temperature of 1100-1300 °C for 1 or more minutes under a non-oxidative atmosphere excluding hydrogen (see column 7, line 10), and subjects the wafer to a heat treatment at a temperature of 700-1300 °C for 1 or more minutes under an oxidative atmosphere.

Subjecting the wafer to a heat treatment at a temperature of 1100-1300 °C for 1 or more minutes under a non-oxidative atmosphere excluding hydrogen serves to eliminate the inner wall oxide films which are caused by grown-in defects (see column 7, lines 15-21). The second heat treatment at a temperature of 700-1300 °C under an oxidative atmosphere is conducted to remove an oxide film which is caused by grown-in defects as well as surface roughness due to the first heat treatment under the non-oxidative atmosphere. The non-oxidative atmosphere is disclosed as being argon, nitrogen, or a mixed gas thereof, but does not contain hydrogen.

With the present invention, by contrast, the first heat treatment is performed at a temperature equal to or higher than 1200 °C under a *non-oxidative atmosphere that contains hydrogen* or an *oxidative atmosphere*, to eliminate grown-in defects. Furthermore, the second heat treatment is performed as rapid thermal annealing for a duration of two minutes or less which makes it possible to produce gettering site through this process.

For at least the foregoing reasons, claims 1, 8, 20 and 25 are neither taught nor suggested by the prior art, but are patentable thereover. Favorable reconsideration is requested. Claims 2-5, 7 and 21-24 are also in condition for allowance as claims properly dependent on an allowable base claim and for the subject matter contained therein. Favorable reconsideration and allowance thereof is requested.

As set forth in amended claim 17, the present invention is also directed to a method of growing an ingot comprising the steps of accelerating a speed of growing from a melt-down silicon to a single crystalline silicon ingot, maintaining a temperature gradient distribution from a central part to a circumferential part of the ingot at a growing interface between the melt-down silicon and the ingot grown by crystallization, forming an OiSF ring at the circumferential part by moving the OiSF ring from a center of a single crystalline semiconductor growth axis to a circumference, and extending an area in which delta (Oi) is increased as compared to that of other areas, wherein the delta (Oi) is a difference between an initial oxygen concentration and oxygen concentration after heat treatment with a thermal history which is carried out at 1000°C for 64 hours in a N_2 ambience.

Generally, though there are differences according to crystal growing conditions, the interior part of a silicon single crystalline is divided into three regions, the vacancy-rich region, the neutral region and the interstitial region. Iida relates to the conditions necessary to produce the neutral region. Any explanation of the process of producing vacancy-rich, neutral and interstitial regions is according to temperature requirement, and there is no teaching that would explain the process of forming the OiSF ring at the circumferential part or removing the OiSF ring by moving

the OiSF ring from the center of a single crystalline semiconductor growth axis to a circumference, nor of extending a particular region in which it is easy to produce bulk micro-defects of high density.

As set forth in claim 17, the present invention relates to the conditions of producing the vacancy-rich region by "forming an OiSF ring at the circumferential part by means of moving the OiSF ring from a center of a single crystalline semiconductor growth to a circumference, and extending an area in which delta (Oi)is greatly increased as compared to those of other areas, with delta being the difference between an intial oxygen concentration and oxygen concentration after heat treatment with a thermal history which is carried out at 1000°C for 64 hours in a N_2 ambience, thereby extending the particular area in which it is easy to produce bulk micro-defect of high density. This is not taught or suggested by Iida.

Nor does Matsushita provide the necessary teaching. Matsushita states methods of eliminating lattice defects like stacking faults by heating the ingot at a temperature of 1000-1200°C for 15 hours. Thus, Matsushita provides a method of producing lattice strains inside the silicon single crystalline and later etching off to produce a silicon single crystalline wafer. This does not teach or suggest the present invention in which a process is claimed that extends an area in which delta (Oi) is greatly increased as compared to that of other areas. Specifically, the heat treatment with a thermal history which is carried out at 1000°C for 64 hours in a N_2 ambience results in the delta (Oi) having increased area. Therefore, unlike Matsushita which is only a heat treatment process as part of an ingot or wafer producing process, the present invention provides a tool for observing a certain area clearly, which facilitates explanation of the wafer producing processes.

For at least the foregoing reasons, claim 17 is allowable over the prior art. Favorable reconsideration and allowance thereof, as well as claim 19 dependent thereon, is requested.

Attached hereto is a marked-up version of the changes made to the application by the current amendment. The attached pages are captioned "Version with Markings to Show Changes Made".

Should the Examiner have any questions or comments, the Examiner is cordially invited to telephone the undersigned attorney so that the present application can receive an early Notice of Allowance.

Respectfully submitted,

JACOBSON HOLMAN PLLC

By Yoon S. Ham by Sag C Seeley
Yoon S. Ham
Reg. No. 45,307
Reg No 40,495

400 Seventh Street, N.W.
Washington, D.C. 20004
Telephone: (202) 638-6666
Date: February 26, 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 18 has been canceled and claims 1, 3, 4, 8 and 17 have been amended as follows:

1. (Twice Amended) A method of treating a wafer thermally to remove defects contained in single crystalline semiconductor, the method comprising the steps of:

carrying out a heat treatment on the wafer at a temperature equal to or higher than 1200 °C under a non-oxidative atmosphere containing hydrogen; and

carrying out a rapid thermal annealing on the wafer at a temperature equal to or lower than 800°C for a period having a duration of two minutes or less.

3. (Amended) The method of treating a wafer thermally according to claim 1, wherein the first heat treatment is carried out at an ambience of one of hydrogen[, inert gas,] and a [first] mixed gas of hydrogen and inert gas[, and a second mixed gas of oxygen and inert gas].

4. (Amended) The method of treating a wafer thermally according to claim 3, wherein flow of the [inert gas, the first] mixed gas[, and the second mixed gas] ranges from 2 to 50 slm.

8. (Twice Amended) A method of producing a semiconductor wafer, comprising the steps of:

producing a single crystalline semiconductor ingot by removing an OiSF ring by means of moving the OiSF ring from a center of a single crystalline semiconductor growth axis to a circumference and by extending a first area and a second area in which delta (Oi) as oxygen concentration difference between initial oxygen concentration and oxygen concentration after heat treatment in N_2 ambience at 1000 °C for 64 hours, is increased more than other areas;

providing a wafer by slicing the single crystalline semiconductor ingot;

carrying out a heat treatment on the wafer at a temperature equal to or higher than 1200 °C <u>under a non-oxidative atmosphere containing hydrogen</u>; and

carrying out a rapid thermal annealing on the wafer at a temperature equal to or lower than 800°C for a period having a duration of two minutes or less.

17. (Twice Amended) A method of growing an ingot, comprising the steps of:

accelerating a speed of growing from a melt-down silicon to a single crystalline silicon ingot;

maintaining a temperature gradient distribution <u>uniformly</u> from a central part to a circumferential part of the ingot at a growing interface between the melt-down silicon and the ingot grown by crystallization;

forming an OiSF ring at the circumferential part by moving the OiSF ring from a center of a single crystalline semiconductor growth axis to a circumference[; and

extending] <u>in order to extend</u> an area in which delta (Oi) is increased as compared to that of other areas, wherein the delta (Oi) is a difference between an initial oxygen concentration

and oxygen concentration after heat treatment with a thermal history which is carried out at 1000°C for 64 hours in a N_2 ambience.